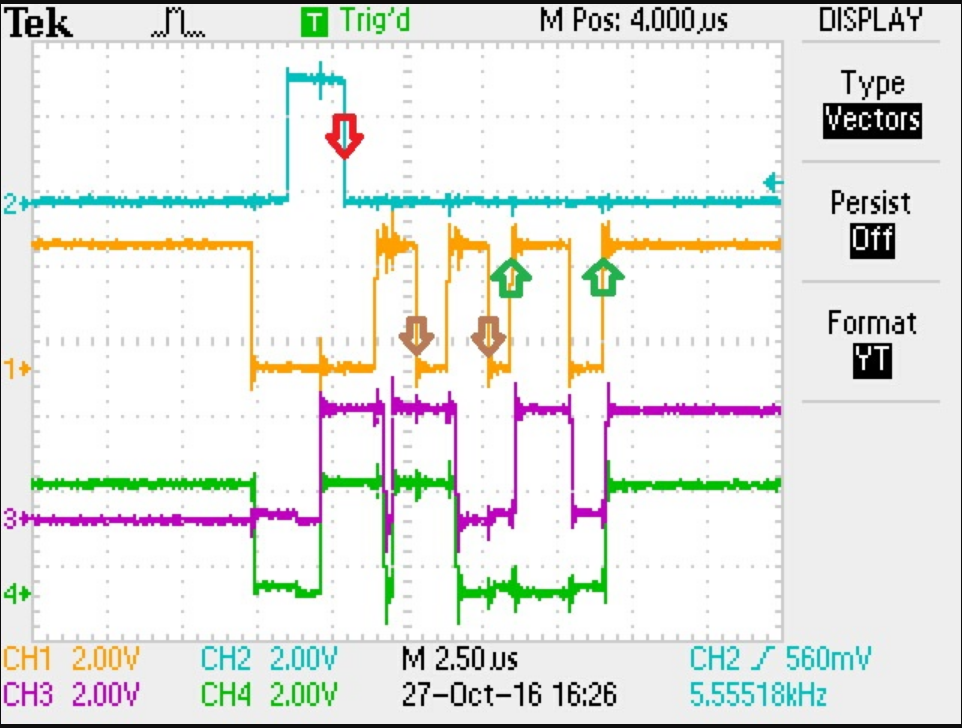
From:

https://www.cnczone.com/forums/dynomotion-kflop-kanalog/320102-kkonnect-kflop.html



Channel:  
1. CLKIN (pin 15).  
2. STARTIN (pin 16).  
3. DB0 (pin 5).  
4. DB1 (pin 6).  
  
Arrows:  
Red - capture address on the falling edge STARTIN.  
Brown - capture output on the falling edge CLK (8х2 = 16 output).  
Green - setting the input value of the data lines on the rising edge CLK( 8x4 = 32 input + 8 check bit). The value of the last input fixedly to check - 0xA5.  
  
Use in the scheme of microcontrollers - not work idea, time delays are too small. If you need an adapter to IO module is necessary to use the FPGA.

From a previous comment

Protocol in the subject, unfortunately, not true.  
Latching addresses and registers on the output registers occurs on the falling edge.  
Does anyone have any information whether at some point there is latching on KFLOP input0-input4?

Hi Smouk,  
  
While the CLK is high the Konnect board drives the data Bus with the current Input Data. After some time KFLOP reads the data (which latches the data) then quickly puts the CLK low.  
  
HTH  
Regards

Regards  
TK